SMC-00-126

December 17, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/671,259 09/25/03

Nai-Yin Sung et al.

A METHOD FOR PROVIDING VITAL MODEL OF EMBEDDED MEMORY WITH DELAY BACK ANNOTATION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 12/19/03

"VHDL Sign-Off Simulation: What Future?," Bakowski, et al., Proceedings of the VHDL International Users Forum, Spring Conference, 1994, IEEE, May 1994, pp. 136-141, describes that a universal VHDL gate library for ASIC sign-off simulation can be developed, even though the optimized VHDL code for various target simulators may differ. The solution is based on VHDL models written with a unique entity declaration and various architecture bodies targeted at simulators, concentrating on VITAL compliant architectures.

"Standardizing ASIC Libraries in VHDL Using VITAL: a Tutorial," Krolikoski, Proceedings of the IEEE 1995 Custom Integrated Circuits Conference, IEEE, May 1995, pp. 603-610, provides an overview of the central features of VITAL Models using several VITAL-compliant styles are presented and discussed.

"IEEE Standard for VITAL Application Specific Integrated Circuit (ASIC) Modeling Specification," Design Automation Standards Committee of the IEEE Computer Society, USA, IEEE Std 1076.4-1995, May 1996, defines the VITAL (VHDL Initiative Towards ASIC Libraries) ASIC Modeling Specification.

U.S. Patent 6,026,226 to Heile et al., "Local Compilation in Context Within a Design Hierarchy," discusses electronic design automation.

DRAFT Standard, VITAL ASIC (Application Specific Integrated Circuit) Modeling Specification, Design Automation Standards Committee of the IEEE Computer Society, IEEE P1076.4/D1, April 2000, IEEE Standards Board, is a proposed standard which defines the VIATL (VHDL Initiative Towards ASIC Libraries) ASIC Modeling Specification. This modeling specification defines a methodology which promotes the development of highly accurate, efficient simulation models for ASIC) Application Specific Integrated Circuit) components in VHDL.

U.S. Patent 5,875,111 to Patel, "Method for Providing a Vital Model of a Pullup/Pulldown Device with Delay Back Annotation," discloses a method of modeling a pullup device and a pulldown device with delay back annotation in accordance with the VITAL application specific integrated circuit modeling specification.

U.S. Patent 6,141,631 to Blinne et al., "Pulse Rejection Circuit Model Program and Technique in VHDL," discloses a method which determines the behavior of a logic cell that receives input signals resulting in a narrow pulse or "glitch."

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

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ASSOCIATE POWER OF ATTORNEY

I hereby appoint Billy Knowles, registration number 42,752, as my associate attorney in this case. His telephone number is (845) 331-3866.

Please continue to direct all correspondence in this case to the undersigned attorney.

Respectfully submitted,

Stephen B. Ackerman,

Principal attorney of record

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-00-126	10/671,259
Applicant Nai-Yin Sung et al.	
Filing Date 09/25/03	**Group Art Unit**

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6026226	2/15/00	Heile et al.	395	500.13	10/27/97
	5875111	2/23/99	Patel	364	488	3/25/97
	6141631	10/31/00	Blinne et al.	703	14	3/25/98

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

—	"VHDL Sign-Off Simulation: What Future?," Bakowski, et al, Proceedings of the VHDL Int'l Users Forum, Spring Conf., 1994, IEEE, May 1994, pp. 136-141.
—	"Standardizing ASIC Libraries in VHDL Using VITAL: a Tutorial," Krolikoski, Proc. of the IEEE 1995 Custom Integrated Circuits Conf., IEEE, May 1995, pp. 603-610.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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	"IEEE Standard for VITAL Application Specific Integrated Circuit (ASIC) Modeling Specification," Design Automation Standards Committee of the IEEE Computer Society, USA, IEEE Std 1076.4-1995, May 1996.

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-	DRAFT Standard, VITAL ASIC (Application Specific Integrated Circuit) Modeling Specification, Design Automation Standards Committee of the IEEE Computer Society, IEEE P1076.4/D1, April 2000, IEEE Standards Board.

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